REMARKS

Claims 1-20 are pending in the present application. Claims 1 and 12 are amended herein. A marked-up copy of the changes to the Claims is attached as Appendix I. The specification has been amended herein to correct typographical errors. A marked-up copy of the changes made to the specification is attached as Appendix II.

On page 4, lines 11-14, and line 35; page 5, line 2; and page 9, line 25, the specification has been amended from "second region" to "first region". The basis for this change may be found, as an example, in the specification as filed in Figure 5 and page 8, line 32 through page 9, line 1.

On page 4, lines 27-30, the specification has been amended from "conductive liner" to "seed layer." The basis for this change may be found, as an example, in the specification as filed in Figure 4, and on page 7, line 15 through line 31.

On page 4, line 32, the specification has been amended from "insulating layer" to "inter-level dielectric." The basis for this change may be found, as an example, in the specification as filed on page 6, line 18 through line 27.

On page 9, line 6, the specification has been amended to remove the phrase "by plasma-enhanced chemical vapor deposition (PECVD) or combinations thereof." This phrase was a typographical error that was inadvertently duplicated within the same paragraph.

On page 9, line 20, the specification has been amended from "second conductive material" to "a third conductive material." The basis for this change may be found, as an example, in the specification as filed in Figure 5, and on page 9, line 26-34.

On page 9, line 22, the specification has been amended from "A" to "The". The basis for this change is grammatical in accordance with the change on page 9, line 20.

No new matter is added in the amendment to the specification or claims herein. The particular references to the specification herein are provided as examples of bases for the amendments made herein. The Applicant makes no assertion that they comprise the only or the best examples of support.

In conclusion, in view of the above, the Applicant respectfully requests that the Examiner allow Claims 1-20 and pass the present patent application to issuance. If the Examiner has any questions, the Applicant invites the Examiner to contact the Applicant's attorney at the phone number below.

Respectfully submitted,

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Appendix I
Marked-Up Copy of the Claims

1. (Amended) A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a wafer having a workpiece;

depositing an insulating layer over the workpiece;

patterning the insulating layer with a plurality of trenches, the insulating layer comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap;

depositing a first conductive layer over the insulating layer within the trenches;

depositing a resist over the insulating layer first regions;

depositing a second conductive material within the insulating layer second region trenches;

removing the resist;

depositing a thin dielectric layer over the insulating layer first [second] region within the first [second] region trenches; and

depositing a third conductive material over the thin dielectric layer within the first [second] region trenches.

12. (Amended) A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a wafer having a workpiece;

depositing an inter-level dielectric over the workpiece;

patterning the inter-level dielectric with a plurality of trenches, the inter-level dielectric comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap, the second region comprising trenches for a plurality of conductive lines;

depositing a conductive liner over the inter-level dielectric within the trenches;

depositing a seed layer over the conductive liner;

depositing a resist over the seed layer [conductive liner];

removing the resist over the seed layer [conductive liner] in the inter-level dielectric second regions, leaving resist over the seed layer [conductive liner] in the inter-level dielectric first regions;

depositing a first conductive material within the inter-level dielectric [insulating layer] second region trenches to form a plurality of conductive lines;

removing the resist;

depositing a MIMCap dielectric over the inter-level dielectric first [second] region within the first [second] region trenches; and

depositing a second conductive material over the MIMCap dielectric within the first [second] region trenches to form a MIMCap top plate.

Appendix II
Marked-Up Copy of the Specification

The paragraph beginning on page 3, line 31 through page 4, line 14:

In one embodiment, disclosed is a method of fabricating a vertical MIMCap, comprising providing a wafer having a workpiece, depositing an insulating layer over the workpiece, and patterning the insulating layer with a plurality of trenches. The insulating layer comprises at least one first region and at least one second region, and the first region comprises trenches for at least one MIMCap. The method includes depositing a first conductive layer over the insulating layer within the trenches, depositing a resist over the insulating layer first regions, and depositing a second conductive material within the insulating layer second region trenches. The resist is removed, and a thin dielectric layer is deposited over the insulating layer first [second] region within the first [second] region trenches. A third conductive material is deposited over the thin dielectric layer within the first [second] region trenches.

The paragraph beginning on page 4, line 15 through page 5, line 3:

In another embodiment, disclosed is a method of fabricating a vertical MIMCap, comprising providing a wafer having a workpiece, depositing an inter-level dielectric over the workpiece, and patterning the inter-level dielectric with a plurality of trenches. The inter-level dielectric comprises at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap. The second region comprises trenches for a plurality of conductive lines. The method includes depositing a conductive liner over the inter-level dielectric within the trenches, depositing a seed layer over the conductive liner, and depositing a resist over the seed layer [conductive liner]. The resist is removed over the seed layer [conductive liner] in the inter-level dielectric second regions, leaving resist over the seed layer [conductive liner] in the inter-level dielectric first regions. A first conductive material is deposited within the inter-level dielectric [insulating layer] second region trenches to form a plurality of conductive lines, and the resist is removed. A MIMCap dielectric is deposited over the inter-level dielectric first [second] region within the first [second] region trenches, and a second conductive material is deposited over the MIMCap dielectric within the first [second] region trenches to form a MIMCap top plate.

The paragraph beginning on page 8, line 32 through page 9, line 21:

The resist 20 is removed, and a thin dielectric layer 26 is disposed over the wafer 10, covering the second conductive material 24 in the second regions 17, and also covering exposed portions of the seed layer 18 in first regions 19, as shown in Figure 5. The thin dielectric layer 26 is preferably conformal and comprises a thickness in a range of between approximately 10 nm to 200 nm, as an example. Preferably, the dielectric material 26 comprises silicon nitride, Ta_2O_5, or combinations thereof [by plasma-enhanced chemical vapor deposition (PECVD) or combinations thereof], deposited by plasma enhanced chemical vapor deposition (PECVD). Alternatively, the thin dielectric layer 26 may comprise other dielectric materials such as SiC, saline oxide, tetraethoxysilane (TEOS), silicon dioxide, silicon nitride, silicon oxynitride, barium strontium titanate (BST) or other insulators, as examples. Preferably, the thin dielectric layer 26 is relatively thin, e.g., 10 nm to 200 nm thick, and is conformal. Thin dielectric layer 26 functions as a capacitor dielectric 26 of MIMCap's in region 19, e.g., thin dielectric layer 26 comprises the capacitor dielectric between the vertical/horizontal MIMCap plates comprised of conductive liner 16/seed layer 18, e.g., the first conductive layer, and a third [second] conductive material 28.

The paragraph on page 7, line 7 through line 9:

A first conductive layer is disposed over the insulating layer 14. The first [First] conductive layer includes a conductive liner 16 and a seed layer 18.

The paragraph beginning on page 9, line 22 through line 34:

The [A] third conductive material 28 is deposited over the wafer 10, as shown in Figure 5. The third conductive material 28 is deposited over the thin dielectric layer 26 to fill the trenches 15 in the first [second] region 19 of the wafer 10. The third conductive material 28 comprises the top plate of vertical MIMCap's in region 19. The third conductive material 28 preferably comprises W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof deposited by PVD or CVD, as examples. The third conductive material may comprise any conducting

material such as a metal, and preferably comprises CVD W or CVD Al. Alternatively, the third conductive material 28 may be formed by plating, for example.